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13. ABSTRACT *(Maximum 200 words)*

The focus of research in this program has been the study of fundamental issues in the design and testing of data conversion interfaces for high-performance VLSI signal processing and communications systems. Because of the increased speed and density that accompany the continuing scaling of VLSI technologies, digital means of processing, communicating and storing information are rapidly displacing their analog counterparts across a broadening spectrum of applications. In such systems, the limitations on system performance generally occur at the interfaces between the digital representation of information and the analog environment in which the system is embedded. Specific results of this research include the design and implementation of low-power BiCMOS comparators and sample-and-hold amplifiers operating at clock rates as high as 200 MHz, the design and integration of a 12-bit, 5-MHz CMOS A/D converter employing a two-step architecture and a novel self-calibrating comparator, the design and integration of an optoelectronic communications receiver front-end in a GaAs-on-Si technology, the initiation of research into the use of an active silicon substrate probe card for fully testing high-performance mixed-signal circuits at the wafer level, and a preliminary study of means for correcting dynamic errors in high-performance A/D converters.

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VLSI Circuits for High Speed Data Conversion

FINAL REPORT

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PROBLEM STUDIED

As a consequence of the increased speed and density that accompany the continuing scaling of VLSI technologies, digital means of processing, communicating and storing information are rapidly displacing their analog counterparts across a broadening spectrum of applications. Moreover, increases in the capacity to process information have stimulated corresponding increases in the demands for communications bandwidth. In general, digital signal processing and communications systems provide enhanced noise immunity, precision and flexibility in comparison with analog alternatives. In addition, they are easier to design and test, and they more effectively exploit progress in automation of the design of digital integrated circuits.

In systems wherein information is represented digitally, the limitations on system performance generally occur at the interfaces between this representation and the analog environment in which the system is embedded. Examples of such interfaces include those between digital and analog electronic signals, as well as between optical and electronic means of representing data. Because digital signals can be processed with virtually arbitrary precision, the emergence of powerful digital signal processors, coupled with increases in the available communications bandwidth, has stimulated the demand for faster and more precise data conversion interfaces. Even as analog/digital and optoelectronic interfaces become a diminishing fraction of the hardware comprising an overall system, they bear an increasing responsibility for the limitations on systems performance.

This research program has focused on studying fundamental issues in the design and testing of high-performance data conversion interfaces for VLSI signal processing and communications systems. Specific areas of exploration include the study of basic circuit functions for digitizing signals with bandwidths above 100 MHz, research into the design of MHz-bandwidth precision A/D converters for applications such as radar imaging and wireless communications, an investigation of monolithic GaAs-on-silicon technology for use in the implementation of optoelectronic receivers in optical fiber communications systems, research into means of fully testing high-speed circuits at the wafer level using a silicon substrate probe card, and the initiation of research into the correction of dynamic errors in high-resolution A/D converters.

SUMMARY OF IMPORTANT RESULTS

High-Speed BiCMOS Comparison and Sampling Circuits

Research in this program has addressed architectural issues, generic circuit functions and technology considerations for the design and implementation of a variety of high-performance data conversion interfaces implemented in VLSI technologies. In part, the program provided for the completion of research into fundamental circuit functions needed for analog-to-digital conversion at rates above 100 MHz. This work culminated in the design of a novel BiCMOS charge-steering comparator that performs 8-bit comparisons at rates as high as 200 MHz and the design of an 8-bit, 200-MHz CMOS sample-and-hold circuit wherein Miller feedback is used to compensate for charge-injection errors in the constituent MOS switches.

The basic function of a comparator is that of providing amplification sufficient to generate digital output levels representative of the polarity of small differences between two analog input signals. This amplification need not be linear nor continuous in time. However, for use in applications such as digitizing video and higher bandwidth signals, the amplification must be accomplished as fast as possible at an economy of power and chip area. Earlier research suggested that among the various approaches to comparator design, the minimum delay and power-delay product could best be achieved by obtaining the required amplification through regeneration. Research into the CMOS implementation of regenerative comparators revealed difficulties such as relatively large input capacitance, poor rejection of common-mode transients at the inputs, and clock feedthrough within the regenerative amplifiers. In response to these limitations we began to explore the use BiCMOS technology for the implementation of high-speed, low-power comparators.

The research into the comparison function led to the successful design and implementation of a BiCMOS comparator wherein MOS sampling switches at the input are combined with a cross-coupled bipolar differential pair that provides regenerative amplification by means of charge steering [1]. During sampling of the inputs, the bipolar pair is held inactive by opening its common emitter node, thus keeping the base currents at zero while the sampled input signals establish an imbalance between the base nodes. The sampled input imbalance is then amplified by using MOS switches and capacitors to transfer a fixed amount of charge through the bipolar pair from their common emitter node to the collector outputs. The bipolar pair dissipates no static power, nor does it drain current from the capacitors on which the input samples are

stored. The collectors of the pair are cross-coupled to the bases by means of ac coupling capacitors.

An experimental implementation of the charge-steering comparator was integrated in a 1-μm BiCMOS technology. The thorough characterization of this prototype demonstrated that it provided comparisons with a resolution of 8 bits at rates as high as 200 MHz. The comparator operates from a single 5-V supply and dissipates only 1.6 mW at the comparison rate of 200 MHz.

While the throughput of high-speed A/D converters is typically limited by the rate at which comparisons can be performed, the signal bandwidth that can be digitized at a specified precision is governed by the speed and precision with which the analog input can be sampled. In fully-parallel (flash) A/D converters, the use of an input sample-and-hold circuit circumvents problems arising from the sensitivity of the conversion to mismatches in clock distribution to a large number of comparators and mismatches in delay through the comparator input stages. In multistep converter architectures, the need for an input sample-and-hold circuit is even more important because of the delays associated with quantizing the input in two or more stages.

In general, open-loop architectures provide the fastest implementation of the sampling function. However, charge injection errors and amplifier offsets in conventional open-loop sample-and-hold circuits appear unattenuated when referred to the input, thereby limiting the precision that can be achieved. In high-speed applications, the need for maximum acquisition bandwidth dictates the use of a large sampling switch together with a small hold capacitance and fast clock transitions. However, these conditions result in large pedestal offsets in the hold mode as a consequence of sampling switch charge injection onto the hold capacitance. Therefore, in order to meet the increasingly stringent performance requirements for high-speed data conversion circuits implemented in VLSI technologies, research in this program was devoted to increasing the precision of open-loop sample-and-hold circuits without significantly reducing the sampling rate or bandwidth. This work led to a new method of improving the resolution of an open-loop sampling circuit without the need for either precision capacitors or an increase in capacitor size.

In the proposed approach to open-loop sampling, the analog input is sampled onto an equivalent hold capacitance that is small during the sampling mode but is increased during the hold mode by means of Miller feedback [2]. An experimental circuit demonstrating this approach was designed and integrated in a 1-μm CMOS technology and was shown to provide an order-of-magnitude reduction in the pedestal offset due to charge injection. The prototype

sample-and-hold circuit is capable of sampling a voltage input at a precision of 8 bits within an acquisition time of 5 nsec.

Self-Calibrating High-Resolution Comparators

Fully parallel, or flash, architectures provide the fastest means of digitizing analog signals. However, since flash topologies require 2^n comparators to achieve n-bit resolution, they are not useful for obtaining a precision of more than 8 or 9 bits. To achieve a resolution of at least 12 bits at the conversion rates above a few MHz, some form of multistep or subranging architecture is typically used. Preliminary results of research in this program suggested that an effective approach to achieving 12-bit resolution at the highest possible speeds was a two-step architecture in which stringent requirements are placed the second-stage comparators in order to ease the demands on the remaining analog circuits. For this reason, considerable effort was devoted to the design of fast, self-calibrating comparators in both CMOS and BiCMOS technologies.

For applications in high-resolution, high-speed data conversion, a self-calibrating comparator was designed and integrated in a 2-μm BiCMOS technology [3,4,7]. In this comparator, low-offset bipolar devices are combined with CMOS offset cancellation. One stage of preamplification is followed by offset storage capacitors and two stages of regeneration. Bipolar devices are used in both the preamplifier and, more importantly, the first regenerative amplifier to minimize their inherent offset due to component mismatch and thereby reduce the gain required in the preamplifier. The first stage of regeneration is accomplished using a charge-steering, emitter-coupled pair of bipolar transistors in a manner similar to that used in the 200-MHz BiCMOS design described above. The experimental implementation of this design employed a fully-differential topology and dissipated only 1.7 mW from a single 5-V supply. It achieved a resolution of 200 μV at a comparison rate of 10 MHz.

A novel fully-CMOS comparator was also designed to achieve resolution on the order of 12 bits at comparison rates of at least several MHz [4,7,8]. In comparison with BiCMOS designs, the large offsets characteristic of CMOS regenerative sense amplifiers present a difficult problem. In conventional CMOS designs the influence of large offsets in the regenerative stages is overcome through the use of a high-gain preamplifier that limits the rate at which comparisons can be performed. This research resulted in a novel comparator topology wherein offsets in both the preamplifier and the subsequent regenerative latch are canceled so as to significantly reduce the demands on the preamplifier. An experimental implementation of the architecture was integrated in a 1-μm CMOS technology at National

Semiconductor and shown to achieve an offset of only 300 μV at a comparison rate of 5 MHz, while dissipating 1.8 mW from a single 5-V supply.

12-bit, 5-MHz CMOS A/D Converter

The self-calibrating CMOS comparator served as one of the essential components in the design of a 12-bit, 5-MHz analog-to-digital converter. This converter is based on a two-step half-flash architecture consisting of a 7-bit coarse flash stage, a 7-bit capacitance D/A converter, a unity-gain subtractor, and a 6-bit fine flash stage. One bit of overlap between the two stages is used to relax the performance required of the first stage comparators, and only the comparators in the second stage need resolve differences as small as 0.5 LSB of the overall converter. Offsets are canceled in both the first and second stage comparators on every comparison cycle. The use of offset cancellation on every cycle serves to attenuate the effect of flicker noise at the comparator inputs.

A fully differential implementation of the two-step A/D converter was integrated in a 1-μm CMOS technology at National Semiconductor. Experimental measurements of this converter confirm that it provides a resolution of 12 bits at sampling rates as high as 5 MHz, while dissipating only 200 mW from a single 5-V supply.

Monolithic GaAs-on-Si for Fiber-Optic Communications

As the demand for communications bandwidth in high-performance systems continues to grow, optical interconnections become increasingly attractive, even for local interconnects and at the board level. However, if optical fibers are to be used for local interconnections, substantial improvements must be made in the transceiver electronics with respect to power dissipation and cost, as well as sensitivity and bandwidth. Progress in the ability to selectively grow epitaxial GaAs films on silicon substrates offers one means of providing such improvements.

The monolithic integration of an optoelectronic photodetector together with a transimpedance receiver offers the potential benefits of increased bandwidth, improved sensitivity, and reduced power dissipation. However, while the optical properties of compound semiconductors make them the materials of choice for optical detectors, silicon is the preferred material for the subsequent processing of electronic signals. The selective growth of GaAs films on a silicon substrate makes it possible to merge GaAs and silicon devices on a common substrate. To explore the potential of such an approach, a monolithic GaAs-on-silicon technology was developed wherein compound semiconductor devices could be formed

on a silicon substrate in a fashion compatible with integration of both bipolar and MOS devices in that substrate.

The research into GaAs-on-silicon technology resulted in the successful design and implementation of an optoelectronic receiver front end in which a GaAs metal-semiconductor-metal photodetector was integrated on a substrate containing a silicon bipolar transimpedance preamplifier [6,9]. Experimental measurements confirm that the GaAs diodes were fabricated without disturbing the characteristics of the underlying silicon devices. The pulse response of the experimental receiver is less than 550 psec FWHM.

In high-bandwidth applications a transimpedance architecture is usually used for the design of optical receiver preamplifiers. However, in conventional transimpedance designs there exists a tradeoff that limits the achievable performance because both the input-referred noise and the receiver bandwidth depend on the feedback resistance. If this resistance is increased to lower the input-referred noise and improve the receiver sensitivity, then there is a corresponding reduction in the receiver's bandwidth. In this research a novel pole-zero cancellation technique was devised whereby the influence of the pole at the input of the preamplifier is greatly reduced. The receiver bandwidth is then no longer inversely proportional to the feedback resistance. The cancellation of the pole at the input of the preamplifier is accomplished by introducing a pole in the feedback network of the transimpedance amplifier that acts as a zero in the amplifier's closed-loop response. The input pole can thus be canceled simply by appropriately positioning the feedback pole.

The input-pole cancellation technique was demonstrated experimentally in the design of a CMOS preamplifier. Two amplifiers, one a conventional design and the other employing input-pole cancellation, were integrated in a 2-μm CMOS technology. Measurements of these circuits confirm that the input-pole cancellation provides more than a factor of three improvement in bandwidth for the same noise performance. Alternatively, for the same bandwidth the sensitivity of the preamplifier can be improved. Although the cancellation technique was demonstrated in a CMOS circuit, it is equally applicable to bipolar and GaAs circuits.

Active Substrate Probe Card

As the internal performance of integrated circuits continues to improve with the scaling of VLSI technology, the penalties associated with driving signals off chip increasingly limit overall system performance. In response to this dilemma, some form of multichip module technology seems likely to become the packaging technology of choice for high-speed digital

and mixed-signal systems. However, MCM packaging requires that circuits be fully tested at the wafer level, prior to package assembly. In conventional test systems this is virtually impossible to accomplish because of the large physical dimensions the system and the associated parasitic components. Therefore, substantial improvements in the interfaces between the device under test (DUT) and the automatic test equipment will be required. In this program we began to explore means of achieving such improvements by placing the "pin" electronics as physically close to the DUT as possible, thereby minimizing the interconnect parasitics between the test electronics and the DUT.

The research in this program focused on improving the accuracy of high-speed testing at the wafer level by integrating active test circuits in a silicon substrate probe card, in close proximity to the die under test. In the initial phase of this research, a high-speed linear buffer was designed, and is being integrated in a prototype silicon substrate probe card, in order to decouple the interconnect loading from the DUT. By matching the output impedance of the buffer to the transmission line of the test system, multiple reflections and the resulting timing measurement errors can be eliminated. The initial buffer design comprises a cascade of two CMOS attenuators, three bipolar emitter followers, and a class AB output stage. Active feedback is used in the output stage to improve its linearity. The circuit is capable of driving 50-Ω transmission lines and is expected to track DUT waveforms with bandwidths as high as 400 MHz.

Calibration of Dynamic Errors in High-Resolution A/D Converters

The resolution of precision A/D converters often degrades with increasing signal frequency, especially for conversion rates approaching the maximum achievable in a given technology. While methods of correcting static errors in precision data converters have found widespread use, it remains unclear as to where similar techniques can be devised for correcting dynamic errors. Therefore, in the final year of this program research was begun into dynamic error correction methods for multistep A/D converters. The initial tasks undertaken in this effort have been research into whether signatures can be found for dynamic errors and an exploration of statistical calibration and modeling techniques for dynamic error correction. In addition, a 12-bit, multistep A/D converter designed at National Semiconductor has been modified in such a fashion as to allow its use in the experimental investigation of dynamic error correction algorithms.

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